

CONTROLLING VOLTAGE TRANSIENTS IN FULL BRIDGE DRIVER APPLICATIONS

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In applications that involve fast switching of inductive loads, designers must consider the voltage transients that are generated in such applications. To insure a reliable design, the voltage transients must be limited to a level that is within the safe operating conditions of the switching device. This application note discusses the sources of voltage transients in full bridge applications and techniques that can be used to limit these over-voltage conditions to safe levels. Special attention will be given to applications using monolithic implementations of full bridge circuits like the SGS-THOMSON L6202 and L6203.

MAXIMUM RATINGS

The maximum voltage rating for the bridge driver can be derived from the maximum ratings of the devices used in the output stage and are generally the BV_{ce0} or BV_{dss} of the power devices. In addition to the maximum allowable voltage across the output device, additional limits may be needed on the maximum output voltage above supply or below ground, depending on the implementation of the output stage.

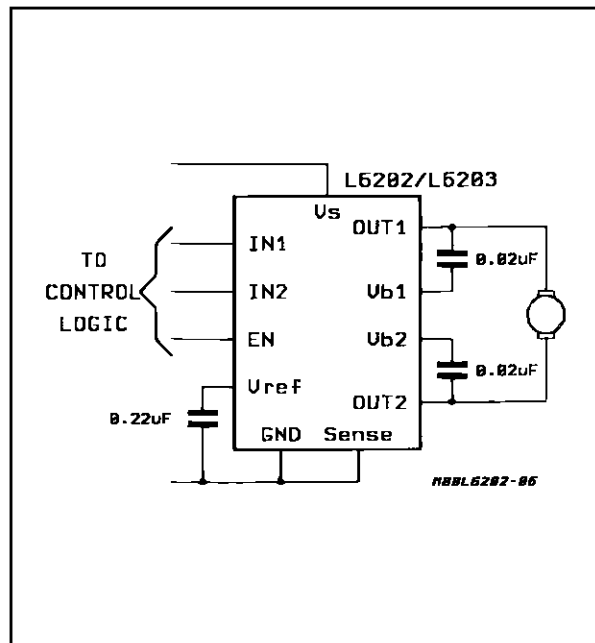
As an example of a full bridge circuit, consider the SGS-THOMSON L6202 and L6203. These devices are full bridge drivers implemented with DMOS transistors on a monolithic structure. Using these devices full bridge drive circuits, like shown in figure 1, are easily implemented. The device has a maximum rating for the supply voltage of 60V, which implies a maximum BV_{dss} for the output devices of 60V. In addition, due to the monolithic implementation, the voltage between the two output terminals must not

exceed 60V. Therefore, the maximum ratings that must be considered for the application are :

V_{supply}	60V
V_{ds} any output	60V
$V_{01} - V_{02}$	60V

Similar maximum ratings will exist for any full bridge application, with the exception of the differential output voltage limit, which will not exist for discrete implementations.

Figure 1 : DC Motor Drive Circuit using L6203.

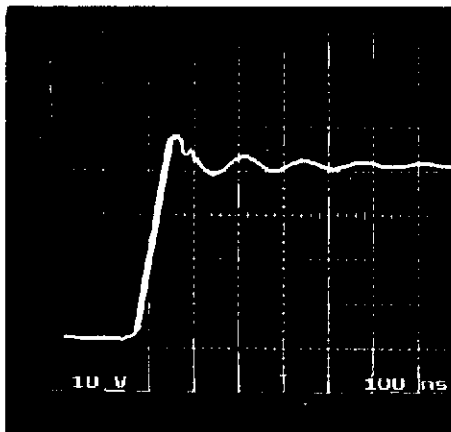


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SOURCES OF VOLTAGE TRANSIENTS

To protect against the over-voltage that may occur as a result of the inductive property of the load, voltage clamps are normally employed to limit the voltage across the output devices. In bridge applications these clamps are normally a diode bridge that clamps the voltage to one diode drop above supply and one diode drop below ground. However, if the diode switches slower than the transistor, there is a short time where neither the transistor nor the diode is conducting and the voltage rise is limited only by the capacitance on the node. The result is that a voltage overshoot occurs during the time before the diode turns on. When the bridge is built with DMOS power transistors, the intrinsic body diode is often used as the clamp. This is true for the L6202 and L6203. As can be seen in the figure 2, the turn-off time of the DMOS device in the L6203 is in the range of 25 to 50nS while the turn-on time of the intrinsic drain to source diode is in the range of 150nS. This difference in switching time is characteristic of many DMOS devices.

Figure 2 : Output Switching Waveform for L6203.

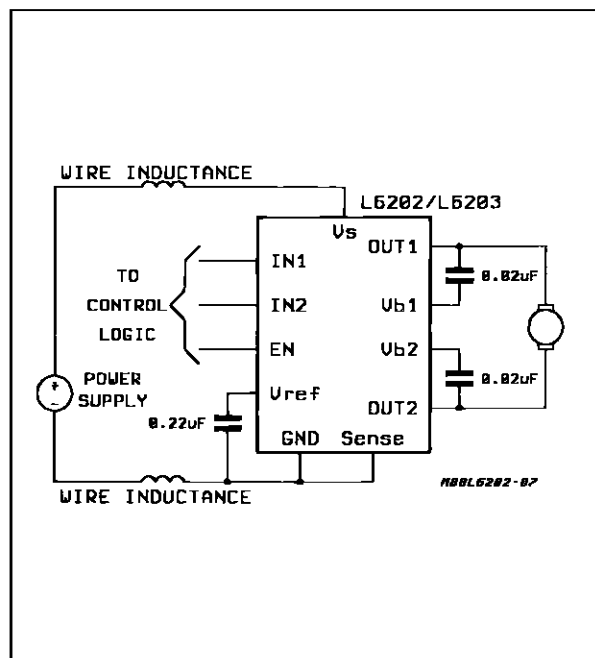


The second main factor contributing to the transients is the parasitic inductance in the wiring or printed circuit board layout. Figure 3 shows the parasitic inductances in the DC motor application. When the

current flowing in these parasitic inductances is rapidly switched, the inductive property of the wire causes a voltage transient. When large currents are rapidly switched, as with DMOS transistors, large voltage transients can be induced across even small parasitic inductances. For an inductive load driven by an H-Bridge the change of current in the power supply lead is equal to twice the load current when the bridge is switched off or the bridge is switched from one diagonal pair of transistors being on the other pair. Here switching the bridge results in a change of direction of current flow in the power leads. The time that it takes to switch the current is essentially the turn off time of the output device. In this case the resulting voltage across the inductance is given by the equation :

$$v = L \frac{di}{dt} = \frac{L_2 \times I_1}{T_{off}} \quad (1)$$

Figure 3 : Parasitic wiring Inductances in DC Motor Drive Circuit.

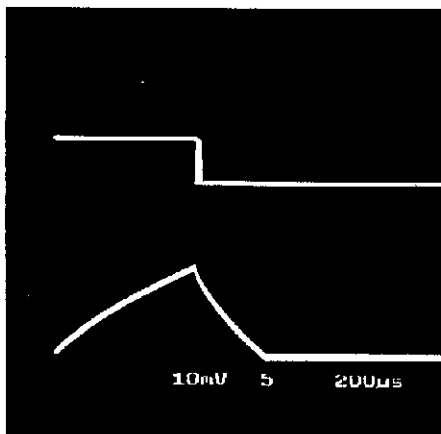


In fast switching applications, like the L6202, where the switching time is as short as 25nS, the induced voltage spike can become quite large. For example if the DC motor in figure 3 was driven with 4A and the bridge was switched off, a parasitic inductance of only 15nH would produce a 5V spike. Since the current is reversed in both the supply and ground leads the device would see a 10V spike between the power supply pin and chip ground, if the inductance of both wires were the same.

As a design example, consider a DC motor driver shown in figure 1 with the following system characteristics :

Supply Voltage	Max 46V Min 38V
Peak Motor Current	5A
Chopping Frequency	50kHz

Figure 4 : Enable Input and Motor Current for Examples.



For evaluation, the motor will be driven with a peak current of 4A. Figure 4 shows the input signals for the L6202 and the motor current used in the evaluation.

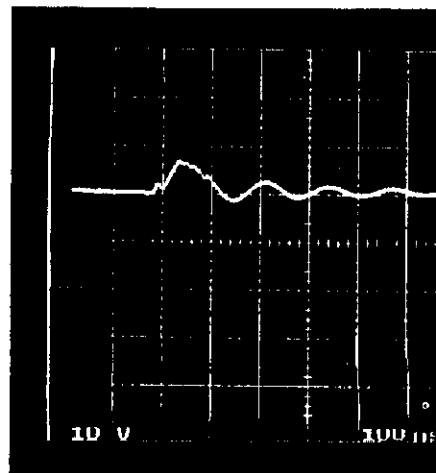
Here the bridge is energized and the load current is allowed to build up to 4A. When the 4A peak is reached, the bridge is disabled and the current decays through the intrinsic diodes in the DMOS power stage. All figures in the remainder of this note are taken under these operating conditions.

POWER SUPPLY FILTERING

To reduce the effect of the wiring inductance a good high frequency capacitor can be placed on the board near the bridge circuit to absorb the small amount of inductive energy in the leads. It should be noted that this capacitor is usually required in addition to an electrolytic capacitor, which has poor performance at high frequencies.

Operating Voltages.

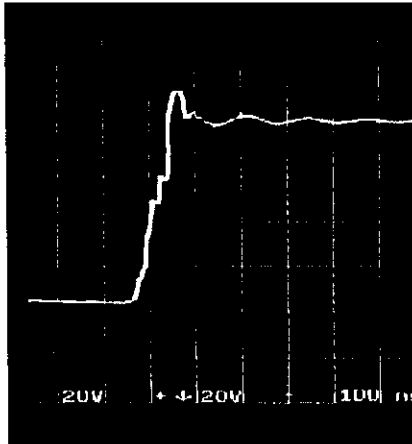
Figure 5a : Supply Voltage.



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Figure 5a shows the spike on the power supply pin of the L6203 and the output pins when the bridge was disabled. These waveforms were present when the device was mounted on a printed circuit board where reasonable care was taken in the layout. When a $0.2\mu\text{F}$ polyester capacitor was connected between the supply and ground pin of the L6203 the voltage spike on the power supply was significantly reduced, as shown in figure 6a.

Figure 5b : V01 - V02.



Looking at the voltage waveform at the output terminals of the L6202, shown in figure 6b, a large spike is still present. The worst case spike is measured between the output terminals of the device ($V_{\text{out1}} - V_{\text{out2}}$) since the spikes above the supply and below ground are both present. After the voltage spike on the power supply was eliminated, the transients on the output must be related to the mismatch of switching times between the diodes and power transistors. To control these spikes two possible alternatives are present ; 1) use faster diodes, or 2) use an external circuit to slow the voltage rise time across the output when the transistors are turned off. Schottky diodes connected external to the L6203 would more closely match the switching time of the DMOS power transistors, but are expensive and require additional board space.

Operating Voltages with $0.2\mu\text{F}$ Bypass Capacitor on Supply Pin.

Figure 6a : Supply Voltage.

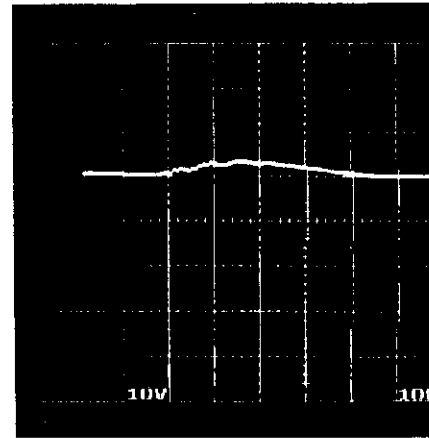
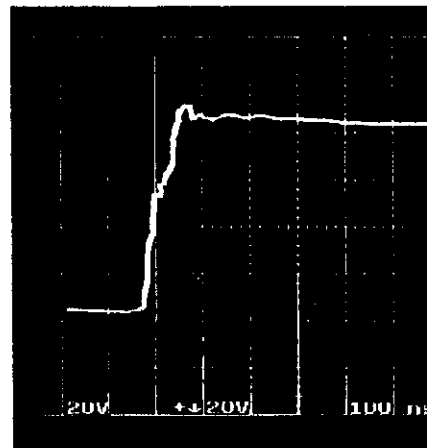


Figure 6b : V01 - V02.

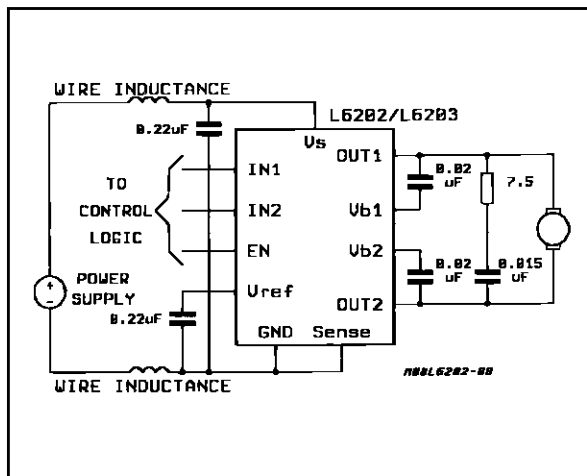


Slowing down the output voltage rise time can be accomplished by connecting a snubber network across the output terminals of the device. Figure 7 shows the connection for a RC snubbing circuit used with the L6203. With properly selected values the slope of the voltage waveform can be limited to where the diodes have sufficient time to turn on and clamp the remaining inductive energy.

SNUBBER DESIGN CONSIDERATIONS

The function of the snubber network is to limit the rate of change of the voltage across the motor (output terminals of the L6203) when one of the DMOS devices is turned off. Using the RC snubbing circuit shown in figure 7, the rate of change of the voltage on the output is dominated by the capacitor while the resistor is used primarily to limit the peak current flowing through the power transistor when it turns on.

Figure 7 : DC Motor Drive Applications with Snubber Network and Bypass Capacitor.



The time constant of the motor current is much longer than the switching time, due to the inductance of the motor. At the time of switching the DC motor can be assumed to be a constant current generator equal to the peak current at switching. If this current

is switched into the snubber, the voltage across the snubber network will jump to a value equal to the snubber resistance times the motor current. After the initial step, the rate of change is limited by the motor current charging the snubber capacitor.

To properly size the snubber network the resistor is selected such that the maximum motor current will produce a voltage less than the minimum power supply voltage. If the resistor is larger than this value, the snubber will be ineffective since the capacitor will not limit the voltage rise until the voltage has become greater than the power supply. For the design example, the maximum resistance for the snubber is given by the equation :

$$R_{max} = V_{smin}/I_{peak} = 38V/5A = 7.6 \text{ Ohm} \quad (2)$$

The snubber capacitor is calculated from the peak current and the target rise time. The capacitance is given by the equation :

$$C = I_{peak} dt/dv = 5A \cdot 150nS/50V = 0.015\mu F \quad (3)$$

When the snubber network is installed in the application the voltage transients on the terminals of the L6203 are greatly reduced, as shown in figure 8.

The drawback of a snubber network of this type is that a current spike will flow into the transistor when it is switched on as the capacitor is discharged. The theoretical peak value of this spike is given by the equation :

$$I = V_{smax}/R = 42V/7.5\text{Ohm} = 5.6A \quad (4)$$

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Operating Voltages with Snubber Network and Bypass Capacitor.

Figure 8a : Supply Voltage.

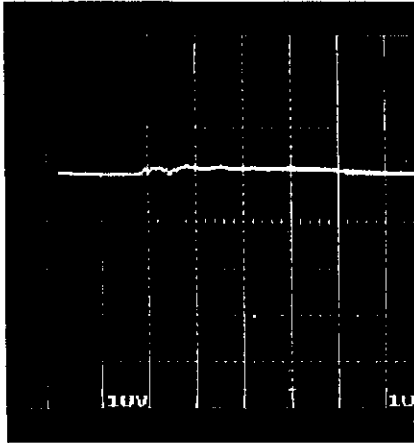
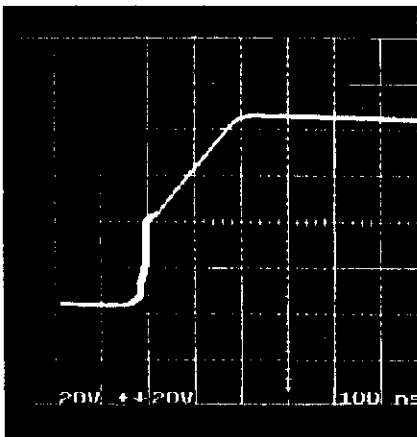


Figure 8b : V01 - V02.

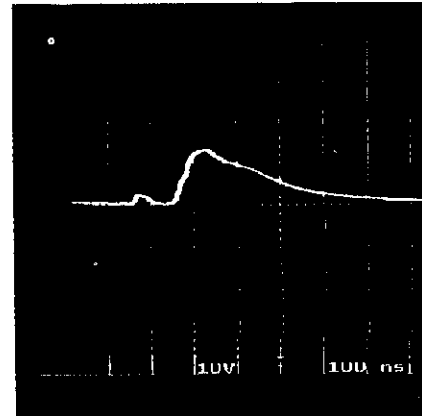


This peak current flowing in the snubber is added to the load current when the device is turned on and the total peak current in the transistor is the sum of

the snubber circuit current plus the load current. In practice the peak current measured is usually much less than the calculated peak, due to the capacitors internal resistance and inductance and the resistor inductance. Figure 9 shows the peak current in the snubber network in the design example.

Current in the Snubber Circuit.

Figure 9a : Turn on 2.0A/div.



The power dissipated in the snubber resistor is the sum of the dissipation during the turn-on and turn-off of the bridge. The resistor dissipation is :

$$P_d = (I_1^2 \cdot R \cdot DC) + (I_2^2 \cdot R \cdot DC) \quad (5)$$

where

I_1 = Current at turn-on

I_2 = Current at turn-off

R = Snubber resistor

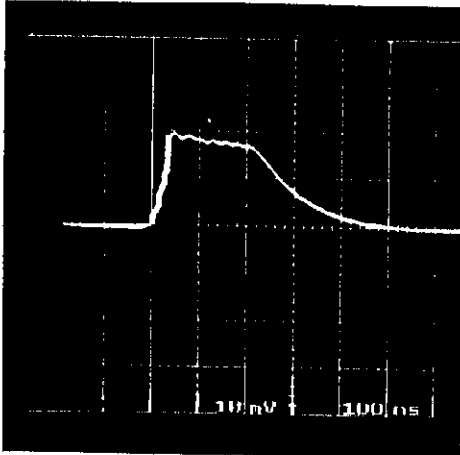
DC = Duty Cycle of current flow

For the design example the power dissipation, not considering the duty cycle is :

$$\begin{aligned} P_d &= ((2.5)^2 \cdot 7.5 \cdot 0.01) + ((5)^2 \cdot 7.5 \cdot 0.01) \\ &= 0.469 + 1.875 \\ &= 2.344 \text{ W} \quad (6) \end{aligned}$$

If the device is chopping for only a portion of the time the dissipation in the resistor will be reduced.

Figure 9b : Turn off 2.0A/div.



CONCLUSION

With the 0.2 μ F bypass capacitor and the snubber circuit in place the voltage transients measured in

the application have been limited to within safe values for the L6202. As shown in figure 8, the power supply voltage, the voltage across each of the DMOS transistors and the voltage across the output of the bridge ($V_{out1} - V_{out2}$) are all within the maximum rating of the device with some margin.

SUMMARY

To insure reliable performance of a H-bridge drive circuit, the designer must insure that the device operates within the maximum ratings of the device(s) used in the circuit. One of the critical parameters to consider is the maximum voltage capability of the devices. To maintain the reliability, the voltage transients due to switching inductive loads must be maintained within the ratings of the device.

Two techniques used to control the voltage transients in fast switching applications are proper bypass filtering of the power supply and snubbing the outputs to control voltage rise times. Using these two techniques the voltage transients in a DMOS bridge application can be controlled to within safe levels.

APPLICATION NOTE

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